Effect of Polymer Gate Dielectrics on Charge Transport in Carbon Nanotube Network Transistors: Low-k Insulator for Favorable Active Interface

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Supporting Information

ABSTRACT: Charge transport in carbon nanotube network transistors strongly depends on the properties of the gate dielectric that is in direct contact with the semiconducting carbon nanotubes. In this work, we investigate the dielectric effects on charge transport in polymer-sorted semiconducting single-walled carbon nanotube field-effect transistors (s-SWNT-FETs) by using three different polymer insulators: A low-permittivity (εr) fluoropolymer (CYTOP, εr = 1.8), poly(methyl methacrylate) (PMMA, εr = 3.3), and a high-εr ferroelectric relaxor [P(VDF-TrFE-CTFE), εr = 14.2]. The s-SWNT-FETs with polymer dielectrics show typical ambipolar charge transport with high ON/OFF ratios (up to ∼105) and mobilities (hole mobility up to 6.77 cm2 V−1 s−1 for CYTOP). The s-SWNT-FET with the lowest-k dielectric, CYTOP, exhibits the highest mobility owing to formation of a favorable interface for charge transport, which is confirmed by the lowest activation energies, evaluated by the fluctuation-induced tunneling model (FIT) and the traditional Arrhenius model (EaFIT = 60.2 meV and EaArr = 10 meV). The operational stability of the devices showed a good agreement with the activation energies trend (drain current decay ∼14%, threshold voltage shift ∼0.26 V in p-type regime of CYTOP devices). The poor performance in high-εr devices is accounted for by a large energetic disorder caused by the randomly oriented dipoles in high-k dielectrics. In conclusion, the low-k dielectric forms a favorable interface with s-SWNTs for efficient charge transport in s-SWNT-FETs.

KEYWORDS: carbon nanotube field-effect transistors, gate dielectrics, polymer dielectrics, conjugated polymer wrapped single wall carbon nanotube, charge transport

INTRODUCTION

Semiconducting single-walled carbon nanotubes (s-SWNTs) are receiving increasing research interest because of their outstanding electrical and optoelectronic properties with excellent mechanical flexibility and chemical stability for a wide range of applications in future transparent, flexible, and wearable devices.1–3 To achieve the large-area devices and inexpensive fabrication desired in production, solution processing is the best method for producing carbon-based electronic devices.4–7 Recently, a selective dispersion of s-SWNTs using various commercially available conjugated polymers has promoted research tremendously.8–12 This method allows for the dispersion of high-purity s-SWNTs (>99%) in organic solvents that are suitable for printing systems.10,13 Due to the advantages of conjugated polymers wrapping s-SWNTs, intensive research has been dedicated to practical applications, not only in logic circuits and light-emitting devices, but also solar cells and organic transistors.7

The gate dielectric has a critical influence on the device performance of field-effect transistors (FETs) because the active channel forms in direct contact with it.16,17
The low-permittivity (eventually removed from the polymers by ultracentrifugation. dodecylthiophene-2,5-diyl) (P3DDT), then enriched and SWNTs were obtained by selective wrapping using poly(3-

The performance of solution-processed s-SWNT-FETs. The s-

poly(methyl methacrylate) (PMMA, relaxor [P(VDF-TrFE-CTFE), fl]

This research has been focused on inorganic dielectrics (e.g., SiO2, ZrO2, and HfO2) produced by atomic layer deposition (ALD).17 The s-SWNT-FETs with polymer dielectrics have been demonstrated as good candidates for the high-performance and flexible-devices approach.16 However, when comparing interfaces of s-SWNTs and inorganic insulators, an understanding of charge transport along heterointerfaces formed by solution processing is desirable. The fundamental understanding of the charge transport therein has received little attention to date.

Here, we study the effects of polymeric dielectrics on the performance of solution-processed s-SWNT-FETs. The s-SWNTs were obtained by selective wrapping using poly(3-dodecylthiophene-2,5-diyl) (P3DDT), then enriched and eventually removed from the polymers by ultracentrifugation. The low-permittivity (εr = 1.8) fluoropolymer (CYTOP, εr = 1.8), poly(methyl methacrylate) (PMMA, εr = 3.3), and ferroelectric relaxor [P(VDF-TrFE-CTFE), εr = 14.2] were chosen for their diverse dielectric constants. All s-SWNT-FETs with polymer dielectrics show typical ambipolar charge transport and high ON/OFF ratios. At the same charge density, the s-SWNT-FETs with CYTOP as the lowest-εr dielectric manifest the highest mobility in both p- and n-channel regimes among all devices studied. The activation energies obtained by using the fluctuation-induced tunneling (FIT) model and the traditional Arrhenius model are also the lowest (EaFIT = 60.2 meV and Eavert = 10 meV), which indicates that the lowest-εr dielectric delivers less disorder to the interface charge transport. The C−F dipole or polar functional groups of the high-εr dielectrics that are randomly oriented near the active interface can limit the charge transport at the interface between s-SWNTs and polymer insulators.

### RESULTS AND DISCUSSION

A top-gate and bottom-contact (TGBC) device structure (Figure 1a) was used for our s-SWNT-FETs, because the active layer could be effectively encapsulated from the environment by the overlying polymer dielectrics to minimize the negative effects from adsorbates (e.g., H2O), which, in turn, can provide a better semiconductor−dielectric interface without air gaps.22 Therefore, this device architecture has the advantage of ambipolar charge transport. The s-SWNTs were selectively dispersed by P3DDT, as introduced by Lee et al., and enriched, and the polymer was eventually removed using ultracentrifugation as reported previously.9,23 The absorption spectrum (Figure 1b) shows 12 kinds of chiralities with a minimal amount of P3DDT (maximum absorption ~460 nm) in the obtained solution. The assignment of chiralities is consistent with the literature.9 The s-SWNTs sorted by P3DDT were analyzed by Raman spectroscopy to confirm the absence of metallic tubes. It was found that the film is composed of only semiconducting nanotubes, as can be verified from the radial breathing mode (RBM) for excitation wavelengths of 633 (Figure 1c), 532, and 785 nm (Figure S1). Generally, the density and length of the s-SWNTs, and the roughness of the film in the channel, have significant influences on the performance of s-SWNT network transistors.1 In our case, the linear density of the s-SWNT network in the FET channel is approximately 22 μm−1 and the average length is 470
nm, as confirmed by transmission electron microscopy (TEM) and atomic force microscopy (AFM) images (Figures S2 and 1d). The root-mean-square (RMS) roughness of the s-SWNT network is approximately 1.57 nm. The chemical structures of the three polymer dielectrics used in this work are shown in Figure 1e. The PMMA and CYTOP films are smooth, pinhole-free, and their RMS roughness is 0.292 and 0.154 nm, respectively, owing to their amorphous nature (Figure S3). The morphology of P(VDF-TrFE-CTFE) shows relatively higher roughness than the amorphous dielectrics, which results from its crystalline nature (Figure S3).

To obtain the precise dielectric capacitance per unit area of the used polymer dielectrics, we employed the effective capacitance ($C_{\text{eff}}$) model suggested by Cao et al., instead of the normal parallel-plate capacitance ($C_{pp}$) mainly used for conventional transistors. In the s-SWNT-network FETs, the parallel-plate model overestimates the gate capacitance, owing to the cylindrical shape of the s-SWNTs and electrostatic coupling between the nanotubes and the gate electrode. For direct estimation of $C_{pp}$ and $\varepsilon_r$ capacitance—voltage ($C-V$) measurements on the metal—insulator—metal (MIM) structure were performed (Figure 1f). Then, we calculated $C_{\text{eff}}$ for the dielectric capacitance per unit area of our s-SWNT-FETs (see section S4 for calculation). In the operation of the transistors, the capacitances showed stable values. It supports the assumption that the application of all the insulators as gate dielectrics is appropriate. In addition, the $C_{\text{eff}}$ are approximately 5.7% lower than the $C_{pp}$ in our system. The thickness and capacitance values are summarized in Table 1.

Table 1. Thickness, Parallel-Plate Capacitance ($C_{pp}$), Effective Capacitance ($C_{\text{eff}}$), and Dielectric Constant of the Polymer Dielectrics Extracted by Measured and Calculated Data

<table>
<thead>
<tr>
<th>thickness (nm)</th>
<th>$C_{pp}$ (nF cm$^{-2}$)</th>
<th>$C_{\text{eff}}$ (nF cm$^{-2}$)</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYTOP</td>
<td>400</td>
<td>3.9</td>
<td>3.7</td>
</tr>
<tr>
<td>PMMA</td>
<td>560</td>
<td>5.2</td>
<td>4.9</td>
</tr>
<tr>
<td>P(VDF-TrFE-CTFE)</td>
<td>500</td>
<td>25</td>
<td>23</td>
</tr>
</tbody>
</table>

$^a$Measured at 10 kHz.

Figure 2 shows the transfer curves of the s-SWNT-FETs with three different dielectrics, which exhibit ambipolar characteristics. The linear and saturation mobilities ($\mu$) were evaluated by the standard formulations (see the Experimental Procedures) with $C_{\text{eff}}$ considered by electrostatic coupling (Table 2 and Table S1). In the FETs with the random network of s-SWNTs as the active layer, the saturation mobility is higher than the linear mobility (Tables 2 and S1). One possible reason is that the hopping barriers of the metal—s-SWNTs contacts and the tube—tube junctions become lower in the saturation regime owing to the strong lateral electrical field. The s-SWNT-FETs with CYTOP and PMMA as low-k insulators show p-type dominant ambipolar characteristics and a higher hole mobility (max. $\sim$6 cm$^2$ V$^{-1}$ s$^{-1}$) than that of the aligned P3DDT-sorted s-SWNT-FET (Figure 3). The devices with P(VDF-TrFE-CTFE) manifest quite high electron mobility (max. 5.81 cm$^2$ V$^{-1}$ s$^{-1}$). The n-channel enhancement of the electron mobility in P(VDF-TrFE-CTFE) devices is attributed to the higher charge density of the channel induced by high $\varepsilon_r$ and low contact resistance ($R_c$) (described below in more detail). The gate leakage current of PMMA devices is the lowest value in operating voltages among the s-SWNT-FETs ($10^{-6}$ A). The s-SWNT-FETs with CYTOP and PMMA gate dielectrics showed 100% yield from 30 and 26 measured devices, respectively. The P(VDF-TrFE-CTFE) devices exhibited a slightly poorer yield of 80% from 13 measured devices.

In ambipolar transistors, the transfer curves generally display a V-shape in the saturation regime ($\text{gate voltage} (V_g) < \text{threshold voltage} (V_{th})$) drain voltage ($V_d$)) because of the overlapping of both hole and electron injections. Accordingly, the ON/OFF ratio of the ambipolar transistor in the saturation regime becomes lower than that in the linear regime (with mostly unipolar transport). Therefore, the ON/OFF ratio is extracted in the linear regime for more accurate and intrinsic properties of s-SWNT-FETs. As shown in Figure 2, the transfer curves of s-SWNT-FETs with various polymer insulators show a high ON/OFF ratio $>10^5$. In the literature, an ON/OFF ratio of FETs with s-SWNT purity $>99\%$ showed approximately 5 orders of magnitude. We speculate that our P3DDT-sorted s-SWNTs are above 99% purity. As shown in Figure 3, which indicated comparison of our devices’ performances with other literature results, the mobilities in our devices are still lower than those of chemical vapor deposition (CVD)-grown s-SWNTs, owing to the small diameter and short length of the s-SWNTs. However, the ON/OFF ratio is much better than that for the other devices.

A large hysteresis at sweep cycling for measuring the transfer characteristics is one of the main problems in s-SWNT-FETs. Generally, this current hysteresis originates from the interface traps distributed between s-SWNTs and the dielectric, as well as the bulk traps in the gate dielectrics. For estimating hysteresis of our s-SWNT-FETs, we define the magnitude of hysteresis as the difference between two $V_d$ at the center of the maximum and minimum drain currents for forward and reverse gate-voltage sweeping. The hysteresis of the devices using low-k dielectrics of PMMA and CYTOP are approximately 3 and 1 V in the linear regime ($V_g = -5$ V), respectively. The hysteresis for the devices using the high-k dielectric of P(VDF-TrFE-CTFE) is approximately 1.4 V in the linear regime ($V_g = -1$ V). Regarding the drain current of devices with CYTOP, PMMA is higher in the forward $V_g$ sweeping (from negative to positive) than in the reverse sweeping (from positive to negative). The devices with P(VDF-TrFE-CTFE), however, show the opposite trend, which is presumably attributed to their ferroelectric properties. We found that the hysteresis of s-SWNT-FETs is relatively insensitive to the dielectric constant of the gate insulators used. Rather, the hysteresis of the devices is more dominantly sensitive to the extrinsic factors (e.g., moisture and ion migration).

As shown in Figure 4, s-SWNT-FETs with different polymer insulators exhibit good output characteristics. It indicates that the polymer insulators are compatible with the s-SWNTs. The low-k devices show sublinear behaviors in n-type output characteristics in the linear region ($V_d < 5$ V), suggesting that the electron injection is limited by the injection barrier. By contrast, the devices with P(VDF-TrFE-CTFE) have good linearity in the linear region.

Because of the differences in the $\varepsilon_r$ and thickness of the dielectrics, a direct comparison among all transistors is not accurate for observation of their intrinsic heterointerface properties between s-SWNTs and dielectrics as well as their bulk traps. Therefore, an expression of the mobility as a function of induced charge density ($Q_{ind}$) in the channel is...
introduced. This expression has been applied to metal oxide transistors by Pecunia et al.36 The induced charge density is determined as $Q_{\text{ind}} = C_{\text{di}}(V_g - V_{\text{th}})$, where $C_{\text{di}}$ and $V_{\text{th}}$ are the gate dielectric capacitance per unit area and the threshold voltage in the linear regime, respectively. Particularly in the same $Q_{\text{ind}}$ region, both the hole and electron mobilities of the devices using low-$k$ dielectrics show significantly higher values than those using high-$k$ dielectrics (Figure 5). It indicates that s-SWNT-FETs with low-$k$ dielectrics can form heterointerfaces with a lower disorder level. The highest electron mobility in the FET with P(VDF-TrFE-CTFE) is owing to high $Q_{\text{ind}}$ (400 nC cm$^{-2}$) induced by the large capacitance from using high-$k$ insulators.

For analysis of the major carrier-type change from low-$k$ to high-$k$ devices, we have evaluated the contact resistance ($R_c$) for each device using the Y-function method37 (Figures 5d and e). In the case of low-$k$ devices, the $R_c$ in the p-channel regime is lower than in the n-channel regime. This is attributed to the hole-injection barrier being lower than that of electron-injection. The valence band (VB) and conduction band (CB) of our sorted s-SWNTs are approximately $-4.8$ to $-5.1$ eV and $-4.0$ to $-4.1$ eV, respectively.38 The difference between the work function ($\Phi$) of the metal electrode (Au, $\Phi = -4.5$ to $-5.0$ eV)12 and the VB of the s-SWNT is similar to, but smaller than, the electron-injection barrier. Conversely, the $R_c$ in the n-channel regime of the high-$k$ incorporated devices is significantly lower than that of low-$k$ dielectrics (Figure 5f).

The temperature dependence of resistances extracted from the transfer curves of the s-SWNT-FETs with diﬀerent dielectrics are shown in Figure 6a. For a fair comparison, we obtained the total resistances at a fixed $|Q_{\text{ind}}| = 129 \pm 2$ nC cm$^{-2}$. The total resistance increases with cooling. This behavior is described by the FIT model proposed by Sheng et al.43,44

Figure 2. Linear (a–d) and saturation (e–h) transfer characteristics of s-SWNT-FETs with various dielectrics ($L = 10 \ \mu m$ and $W = 1000 \ \mu m$). The solid and dotted lines represent the drain current ($I_d$) and gate leakage current ($I_g$), respectively.
\[ R \propto \exp \left( \frac{E}{kT} \right) \]  

(1)

where \( R \) is the sheet resistance, \( T \) is the absolute temperature in Kelvin, \( T_1 \) is the temperature required for an electron to pass through the insulating gap and is thus related to the activation energy, and \( T_0 \) is the temperature above which thermally activated conduction over the barrier begins to occur. The \( T_0 \) and \( T_1 \) are shown in Table S2. The activation energy extracted from the FIT model (\( E_{\text{FIT}} \)) is calculated from the Boltzmann constant \( (k_B) \times T_1 \). We find that charge transport in s-SWNT-network FETs depends strongly on the \( \epsilon_i \) of the used polymer dielectrics. The \( E_{\text{FIT}} \) tends to increase with the \( \epsilon_i \) of the gate dielectrics, indicating the high-\( k \) dielectrics strongly interfere with charge transport in the transistor channel. We also calculated \( E_{\text{FIT}} \) in the n-channel regime, whose trend is the same as that in the p-channel regime (Figure S5). In addition, we calculated the activation energy (\( E_{\text{Ar}} \)) from the Arrhenius model, which corresponds to charge transport via thermally activated hopping (Figure 6b). The trend of \( E_{\text{Ar}} \) is also very similar to the one extracted by the FIT model. The s-SWNT-FETs with low-\( k \) dielectrics (CYTOP and PMMA) showed lower \( E_{\text{Ar}} \) (10–50 meV) than those with high-\( k \) dielectrics (209 meV).

The polar environment around s-SWNTs can influence charge transport. In fact, the charge transport in the network of the s-SWNTs can be explained by the interplay between the intrinsic charge transport in individual nanotubes (intratube charge transport) and charge carrier transport in tube–tube junctions (intertube charge transport). Because the latter is the more dominant charge transport in the s-SWNT-FETs, we focus on the intertube charge transport. Perebeinos et al. reported that surface phonons on polar substrates limited charge carrier transport along the inner individual tube, which resulted in a decrease of the low-field mobility by an order of magnitude from the intrinsic value. Similar results in single-crystal organic transistors whose channel consisted of conjugation-like s-SWNTs have also been reported by Huela et al. They found that high-\( k \) and polarizable dielectrics induced localization of charge carriers. Interestingly, the limited charge transport in both cases is related to the formation of Fröhlich polarons (self-trapping). Likewise, the intratube charge transport in the s-SWNT-FETs with P(VDF-TrFE-CTFE) can be restricted by Fröhlich polarons. In addition, randomly oriented dipoles in high-\( k \) polymer dielectrics can also hinder intertube charge transport which is dominant in our s-SWNT-FETs. Assuming the density of states (DOS) of the s-SWNT network forms the standard deviation of a Gaussian-like distribution in energy (originally, a s-SWNT forms a spike-like DOS due to the 1-D shape of the s-SWNT, by van Hove singularity), the dipolar disorder model suggested by Veres et al. can be applied to s-SWNT network transistors. We also performed mobility calculations based on the Kubo–Greenwood integral that was developed for the charge transport in noncrystalline semiconductors. Interestingly, the calculated mobilities are in good agreement with the experimental results, which indicates that the intertube transport by thermal activation as a major transport mechanism in our s-SWNT-network FETs is similar to hopping in amorphous semiconductors (see section S7 for calculation). The calculations reveal an important fact that the randomly oriented dipoles in high-\( k \) polymer dielectrics near the channel of s-SWNT-FETs can restrict intertube charge transport. Therefore, both

![Table 2. Fundamental Parameters of TGBa SWNT-FETs](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \mu ) [cm²/V·s]</td>
<td>10–100</td>
</tr>
<tr>
<td>( V_m ) [V]</td>
<td>10–100</td>
</tr>
<tr>
<td>( \rho ) [Ω·cm]</td>
<td>10–100</td>
</tr>
<tr>
<td>( d ) [nm]</td>
<td>10–100</td>
</tr>
<tr>
<td>( \epsilon_i ) [ε]</td>
<td>10–100</td>
</tr>
<tr>
<td>( T ) [K]</td>
<td>10–100</td>
</tr>
<tr>
<td>( E_{\text{FIT}} ) [meV]</td>
<td>10–100</td>
</tr>
</tbody>
</table>
intratube and intertube charge transport in s-SWNT-FETs are limited by the polar environment of the high-\(k\) dielectric. The restriction of intertube charge transport is more severe than intratube charge transport. To attain the best device performance, a low-k dielectric appears to be critical.

The dependence on \(\varepsilon_r\) in s-SWNT-FETs is relatively weaker than that of organic FETs (OFETs). In OFETs, the change of mobility spans several orders of magnitude. The localization of charge carriers in the s-SWNT network induced by disordered dipoles can be milder than that in organic

Figure 3. ON/OFF ratio versus mobility graph of SWNT-FETs fabricated by CVD and solution-process. The on/off ratios and mobilities in this work are the maximum values.

Figure 4. Output characteristics of s-SWNT-FETs with various dielectrics. P-type (a, c, e) and n-type (b, d, f) output curves in devices with PMMA, CYTOP, and P(VDF-TrFE-CTFE).
semiconductors because the electronic states of the s-SWNT network are more extended than that of organic semiconductors. The mobility dependence on $\varepsilon_r$ is derived from the coupling between the charge carrier and the polar functional group in high-$k$ insulators, which is more severe in organic semiconductors with charge carriers having higher effective mass. The effective mass of s-SWNTs is expected to be much lower than that of organic materials. Therefore, s-SWNT-FETs indicate a weaker mobility dependence on $\varepsilon_r$ than that of OFETs.

Interestingly, we found that the operational stability of s-SWNT-FETs was closely related to interface charge transport. In general, the gate dielectric plays important roles in stability testing of transistors. The bias stress responses of the s-SWNT-FETs with different dielectrics were measured in hard conditions ($V_g = V_d = \pm 40$ V for low-$k$ dielectrics and $V_g = \pm 15$ and $V_d = \pm 10$ V for high-$k$ insulators, at a prolonged duration of 5 s over a time interval of 1000 s) (Figure 7). In the p-channel regime, the normalized $I_d$ for CYTOP and PMMA dielectrics decayed by $\sim 14\%$ and $\sim 33\%$, respectively, after a 1000 s stress from their initial values. On the other hand, s-SWNT-FETs with P(VDF-TrFE-CTFE) displayed a large increase of normalized drain current by $\sim 70\%$. The $\Delta V_{th}$ of the devices with CYTOP, PMMA, and P(VDF-TrFE-CTFE) are $-0.26$, $-1.72$, and $60$ V, respectively, which follows the same trend as the drain current decay. In the n-channel regime, the normalized $I_d$ of CYTOP and PMMA devices decreased by $\sim 51\%$ and $\sim 70\%$, respectively. The P(VDF-TrFE-CTFE) samples also showed a decrease of normalized $I_d$ by $\sim 85\%$.

The operational stability of the majority carrier is better than that of the minority carrier. The operational stability of s-SWNT-FETs with low-$k$ insulators is considerably better than those using high-$k$ dielectrics. The reason for the $V_{th}$ shift in the ON state is owing to the trapping of mobile charge carriers in pre-existing or stress-generated deep localized states in the semiconductor or dielectrics, or at their interface. In our case, the charge trapping occurred much more in the high-$k$ insulators or the active interface than in the low-$k$ materials. This is believed to be owing to DOS broadening by the randomly oriented dipole moments in the gate insulators.

**CONCLUSION**

In summary, the interface charge transport of s-SWNT-FETs with different polymer insulators has been investigated. The $E_t$ extracted from the thermal charge transport models (FIT and Arrhenius) increase as the $\varepsilon_r$ increases, which indicates that low-$k$ dielectrics form more favorable interfaces between s-SWNTs and dielectrics than the others. The trend of mobilities
and operational stability are in good agreement with that of interface charge transport evaluated by low-temperature measurement. The randomly distributed dipoles in high-k insulators near the active interfaces in fluence the electronic structure of s-SWNTs. We believe that the fundamental understanding of solution-processed s-SWNT networks is crucial for future progress in achieving high-performance carbon-based electronics with disorder-free interface charge transport.

**EXPERIMENTAL PROCEDURES**

**Preparation of P3DDT-Sorted s-SWNTs Solution.** P3DDT (20 000 ≤ \( M_n \) ≤ 50 000 g/mol) and s-SWNTs grown by the HiPco process (diameter 0.8–1.2 nm, purified <13 wt % iron) were purchased from Rieke Metals, Inc., and Unidym, Inc. All other chemicals were purchased from Sigma-Aldrich. The toluene solution of P3DDT (0.7 mg/mL) was prepared and heated at 80 °C for 1 h for complete dissolution. After the solution was cooled, the SWNT powder was added at 0.5 mg/mL, and the solutions were homogenized in a probe tip sonicator (VCX-130, 130 W Ultrasonic Processor) for 1 h at 20 °C. Then, the solution was centrifuged at 199 000g for 1 h (separation of s-SWNTs) and the supernatant was further ultracentrifuged at 320 000g for 10 h (removal of free polymer) (Vision Scientific Inc. VS-65 ultracentrifuge, V1308Ti fixed rotor). The resulting pellets were washed several times for remaining polymer and collected. The enriched and collected pellets were redispersed in toluene using bath sonication.

**Device Fabrication.** Interdigitated source/drain electrodes on Corning Eagle 2000 glass substrate were patterned by photolithography, thermal evaporation of 5 nm-thick nickel and 15 nm-thick gold, and lift-off. The substrates were cleaned in an ultrasonic bath with deionized water, acetone, and 2-propanol for 10 min each. All fabrication processes were performed in an N₂-filled glovebox. The s-SWNT solution was spin-coated onto the substrate at 700 rpm five times and the channel regions of the s-SWNT film were patterned by lift-off technique of photolithography with acetone. The s-SWNT film was annealed at 310 °C for 1 h on a hot plate to remove residual solvent and moisture. For the dielectrics of s-SWNT-FETs, the CYTOP solution (CTL-809M, Asahi Glass) was diluted with the solvent (CT-solv.180) to have a solution:solvent volume ratio of 2:1. The PMMA (\( M_w = 120 \) kDa) was used without further purification and dissolved in n-butyl acetate (80 mg/mL). P(VDF-TrFE-CTFE) (68/28/9 mol %, Solvay) was dissolved in butanone (50 mg/mL). The dielectric solution was spin-coated on top of the s-SWNT films at 2000 rpm for 60 s. The CYTOP and PMMA were baked at 100 and 80 °C, respectively, for 30 min. The devices with P(VDF-TrFE-CTFE) were briefly baked on a hot plate (60 °C, 10 min). Finally, aluminum gate electrodes were thermally evaporated through shadow masks in a high-vacuum chamber (≈10⁻⁷ Torr).

**Characterization.** For sample preparation for Raman spectroscopy, the s-SWNT/P3DDT solution was drop casted several times on a 300 nm SiO₂ wafer. The resulting s-SWNT/P3DDT was annealed on a hot plate (310 °C, 1 h). The Raman spectra were obtained using an inVia confocal Raman

![Figure 6](image-url)
microscope (Renishaw) and LabRAM HR UV/vis/NIR (HORABA). UV–vis–NIR spectra were measured using a PerkinElmer Lambda 750 instrument. The FET electrical characterizations were carried out using a semiconductor parameter analyzer (Keithley 4200-SCS) in an N₂-filled glovebox. The capacitance values of the dielectrics were also measured utilizing a Keithley 4200-SCS connected with an Agilent 4284A LCR meter. The area of the MIM structure was 200 μm × 200 μm. The linear and saturation mobilities were evaluated by the standard formulas: 

\[ \mu_{\text{lin}} = \frac{dI}{dV} \frac{1}{WCG} \]  

and 

\[ \mu_{\text{sat}} = \frac{2I}{WC} \times \left( \frac{dI}{dV} \right) \].

The height and phase images of the s-SWNTs and dielectric films were obtained using an atomic force microscope (Nanoscope III, Veeco Instruments, Inc.) at the Korea Basic Science Institute (KBSI).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.6b06882.

Raman spectra, TEM and AFM images of s-SWNTs, calculation details for capacitance and mobility calculation of s-SWNT-FETs (PDF)

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Notes

The authors declare no competing financial interest.

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