Many attempts have been made to realize a universal memory,[7] that is, an ideal memory device comprising new, fast, non-volatile, inexpensive methods for storing information. Compared to its inorganic counterparts, organic memory has attracted a great deal of interest because of its remarkable progress in organic electronics and its unique advantages: it is inexpensive, lightweight, and capable of printing ubiquitous components onto plastic substrates.[2–4] In an attempt to create a novel organic memory, several types of memory devices based on organic and polymeric materials have been evaluated, including organic electrical bistable devices,[5] organic–inorganic hybrid memory using a polymeric fuse,[6] and organic field-effect transistors (OFETs) based on ferroelectric gate insulators and chargeable gate dielectrics.[7–11] Among these types of organic memory devices, a memory element based on FETs is especially attractive because of its non-destructive readout and single-transistor applications.[12] In this case, the functionality arises from the field-effect modulation by the spontaneous polarization that occurs in ferroelectrics or the trapped charges in chargeable dielectrics, which are referred to as electrets.

While an OFET memory has many potential advantages, state-of-the-art results of OFET memory devices are in a less favorable position, compared to other types of organic memories.[7–11] With respect to the case of organic ferroelectrics, Naber et al. recently demonstrated an on/off ratio of 10^4 with a programming time of 0.3 ms and a memory effect stability of more than one week.[8] However, when compared to ferroelectrics, only a small amount of attention has been given to electret-charged OFET memory, in spite of the similar field-effect modulation. Moreover, the characteristics of OFET memory based on electrets are less well understood than those of ferroelectric-based OFET memory devices due to a lack of research. Katz et al. demonstrated an OFET memory with a polarizable gate insulator that induced a floating-gate-like behavior,[9] and Singh et al. also demonstrated an OFET memory using poly(vinyl alcohol) as a gate electret.[10] However, these devices still do not sufficiently satisfy the criteria demanded in order to compete with other types of memory devices.[13] Furthermore, details of the operating mechanisms of these devices are not well understood. Therefore, the mechanism should be further investigated to successfully develop a high-performance OFET memory based on electrets.

In this Communication, we report on OFET memory devices built on silicon wafers and based on films of pentacene and an SiO_2 gate insulator that are separated by a thin layer of poly(α-methylstyrene) (PaMS), which acts as a polymeric gate dielectric. This OFET memory device displayed reversible shifts in the threshold voltage (V_{Th}) when an appropriate gate voltage (V_g) was applied above a certain threshold via a relatively short switching time. Based on these reversible shifts in V_{Th}, a non-volatile organic memory was demonstrated that takes advantage of the simple configuration of a typical OFET. This device showed a large memory window (about 90 V), a high on/off ratio (I_{On}/I_{Off}) (10^5), a short switching time (less than 1 μs), and a long retention time (more than 100 h). These memory characteristics were obtained only when an appropriate polymeric gate electret layer (e.g., PaMS) was inserted between the SiO_2 gate insulator and the pentacene channel in the typical OFET structure. Therefore, it is possible that this behavior originates from the modulation of the gate field by stored charges in the polymeric gate electret. Detailed reasons for these results and a possible operating mechanism for our OFET memory device are discussed.

A cross-sectional view of the fabricated device structure is shown in Figure 1a. Further details concerning the fabrication of this device are discussed in the Experimental section. Figures 1b and c show the output and transfer characteristics of the devices, respectively. The results indicate reasonably good OFET behavior, suggesting the additional PaMS layer does not degrade the performance of the devices.[14] From the conventional characterization equation,[15] the measured values of the typical field-effect mobility (μ_{FE}), V_{Th}, and I_{On}/I_{Off} were 0.51 cm^2 V^{-1} s^{-1} (maximum value, 0.89 cm^2 V^{-1} s^{-1}), −19 V, and 10^5, respectively. These transistor properties could be further improved by optimizing the growth conditions for the pentacene thin film.[16]
Figure 2a shows shifts in the transfer curve for this OFET memory device after applying an appropriate $V_g$ within a relatively short time (ca. 1 $\mu$s). The entire transfer curve was substantially shifted in the positive direction when a large gate bias of $V_g = 200$ V was applied for 1 $\mu$s, and it was then steadily sustained at the shifted position during subsequent $V_g$ sweeps. As a result, both $V_{Th}$ and the onset voltage ($V_{On}$) of the OFET memory device were changed by more than about 90 V. On the other hand, the shifted transfer curve returned to its initial position when a reverse gate bias of $V_g = -100$ V was applied for 1 $\mu$s. In addition to the positive direction shift, the transfer curve could also be substantially shifted in the negative direction by a reverse gate bias, as depicted in Figure 2b. From these results, it was determined that the values of $V_{Th}$ could be reversibly controlled by using an appropriate gate bias, causing a dramatic change in the drain current ($I_d$) by an order of five at zero gate bias conditions ($V_g = 0$ V). Figure 2c presents the reversible switching behavior of the $I_d$ in a series of programming ($V_g = 200$ V, $V_d = 0$ V; $V_d =$ drain voltage), reading ($V_g = 0$ V, $V_d = -30$ V), and erasing ($V_g = -100$ V, $V_d = 0$ V) processes. Therefore, this device could be utilized as a non-destructive OFET memory because destructive pulses of $V_g$ are not required for sensing the different current states in a range of memory windows.

In this OFET memory, the high operating voltage needed for programming and erasing can be reduced remarkably either by decreasing the thickness of the insulating layer or by using a high-dielectric-constant (high-$k$) layer. In fact, most of the potential drop occurred in the 300 nm thick SiO$_2$ layer. Thus, when an OFET memory device was fabricated using a 100 nm thick SiO$_2$ layer, the operating voltages for programming and erasing were reduced to 60 and $-50$ V, respectively. As can be seen in Figure 2d, this device also showed reliable shifts in transfer characteristics.

The PuMS layer in our OFET memory device is important for memory operation. When a pentacene OFET device was fabricated without a PuMS layer, no significant shifts in $V_{Th}$ were observed under the same gate bias conditions that were used in the previous experiments. This device merely exhibited a degradation in OFET properties such as $I_{on}$, $\mu_{FET}$, and $I_{on}/I_{off}$ showing little shift in $V_{Th}$ (less than 5 V), which may have been caused by bias-stress effects. Therefore, this result suggests the shifts in $V_{Th}$ in the OFET memory device originated from the additional PuMS layer, either via dipolar polarization or charge trapping in the PuMS. However, our results cannot be explained by a dipolar polarization mechanism in PuMS because of its weak polarity and its nearly symmetrical chemical structure. In addition, the device showed only weak hysteresis behavior between the upward and downward scans for the transfer curve (not shown here). Thus, the trapped charges at the interface between pentacene and PuMS have little effect on the memory characteristics in our OFET memory device. The shifts in $V_{Th}$ after the programming process are therefore thought to be due to the effect of trapped charges in the PuMS layer via charge transfer between the pentacene and the PuMS layer. This result indicates that the additional PuMS gate dielectric layer behaves as a polymeric gate electret, similar to a floating gate in a flash memory.

The number of transferred charges ($\Delta n$) can be determined from the shift in $V_{Th}$ after the programming process, according to

$$\Delta n = \frac{\Delta V_{Th} C_1}{e}$$

where $e$, $\Delta V_{Th}$, and $C_1$ are the element charge, the shift in $V_{Th}$, and the capacitance of the gate dielectric, respectively. From this relation, the surface density of charges transferred from pentacene to PuMS, $\Delta n$, was estimated to be $5 \times 10^{12}$. This value was similar in OFET devices that had both 300 and 100 nm thick SiO$_2$ layers, indicating that the number of trap states in the PuMS layer was nearly constant. This result also provides an explanation for the smaller $V_{Th}$ shift in the 100 nm thick SiO$_2$ device (ca. 30 V) compared to the 300 nm thick SiO$_2$ sample (ca. 90 V), as depicted in Figure 2a and d.
A variety of studies attempting to understand charge-storage and -transport phenomena in electrets have been reported, including examples investigating polystyrene. In these reports, hydrophobic polymers and polymers containing substituted styrenes were found to be good charge-storage media. Thus, P$_{a}$MS might also be a candidate for an effectively chargeable dielectric based on the similar chemical structure of the molecule. This behavior would make the reversible shifts in $V_{Th}$ in this OFET memory reasonable.

Similar OFET memory characteristics were also obtained when polystryene was used as an electret layer; however in this case, performance, such as memory window, was not as good as in the devices using P$_{a}$MS. The reason for this discrepancy is not clear, and further detailed investigations are currently under way.

Although the exact mechanism for charge transfer and trapping in P$_{a}$MS in our OFET memory device is not precisely understood at this time, we offer a potential mechanism, which is schematically shown in Figure 3. When mobile hot carriers are field-generated in pentacene near the interface, they are transferred into the polymer by the transverse electric field. In this model, the applied transverse electric field simultaneously facilitates charge transfer by reducing the effective thickness of the potential barrier at the interface.

The sample was illuminated with visible light during the programming process; after that phase, $V_{g}$ was re-swept without illumination to measure the transfer characteristics. As a result, the critical $V_{g\text{,prog}}$ was dramatically reduced to about 35 V, and beyond that value, a linear change in $V_{Th}$ was observed with increasing $V_{g\text{,prog}}$. In this way the energy barrier is lowered, and the charge transfer between pentacene and P$_{a}$MS can be enhanced.

In addition to the programming and erasing capabilities, the retention time of on- and off-current states is important for
practical applications in memory technology. The retention characteristics of this OFET memory device are shown in Figure 5. Both on- and off-current states were measured at time intervals of 60 s at \( V_g = 0 \) V and \( V_d = -30 \) V in the dark after applying a programming and erasing bias of \( V_g = 200 \) V and \( V_g = -100 \) V for 1 \( \mu s \), respectively. The time required for the on-current state to decrease to 50\% of its initial value, the retention time, was estimated to be more than 100 h by extrapolation of the obtained on-current state curve. In this retention test, a decay of the on-current state showed further non-exponential characteristics: a relatively strong initial decay and a subsequently slower decay. This phenomenon was in good agreement with the model for long-term trapped-charge decay in most experimental studies employing electret materials.[22] From that model, it could be demonstrated that the deeply trapped negative charges are compensated by relatively mobile intrinsic holes until the holes are nearly exhausted, resulting in a comparatively steep initial decay, which is almost exponential in shape. After that, a slow generation of the carrier pairs present in the dielectric continues to supply a small number of holes, which gradually compensate the remaining deeply trapped negative charges, resulting in a slow linear decay.

The retention characteristics of this OFET memory device were also markedly changed when the samples were illuminated with visible light. The decay of trapped charges was much more rapid, and therefore, the retention time for the on-current state was also dramatically decreased. In this case, the trapped charges may decay either from the direct excitation of trapped charges or by compensation of mobile charges generated by illumination. Hence, this photoinduced relaxation could also indicate that charge trapping occurs in the PaMS layer.

In conclusion, an OFET memory device based on pentacene was fabricated using an additional polymeric gate dielectric layer, the electret, which has charge trapping ability. This device showed excellent non-volatile OFET memory characteristics: a high \( \mu_{T}\) above 0.5 cm\(^2\) V\(^{-1}\) s\(^{-1}\), reversible shifts in \( V_{Th} \) by an electrical programming and erasing process within a relatively short switching time of less than 1 \( \mu s \), a long retention time of more than 100 h, and a large memory window of about 90 V. These characteristics are believed to originate from the stored charges in the PaMS layer transferred from the pentacene organic semiconductor to the PaMS polymeric gate electret. After further investigation and optimization, OFET memory devices with these large reversible shifts in \( V_{Th} \) and short switching times could be applied to a variety of potential applications, including novel, non-volatile organic memory, which would be useful for low-cost, lightweight, flexible, low-duty data-storage media and display driver logic.[25]
Experimental

Both pentacene and PuMS (number-average molecular weight \( M_n = 4000 \), glass-transition temperature \( T_g = 76 \)°C) were purchased from the Sigma–Aldrich company and were deposited without further treatment. A thin PuMS layer (ca. 70 nm) was evaporated onto the 100 nm thick \(( C_i = 30 \text{nF cm}^{-2})\) or 300 nm thick SiO\(_2\) \(( C_i = 10 \text{nF cm}^{-2})\) surface of a heavily doped n-type silicon wafer via a spin-coating process using a 1.0 wt % solution in toluene, and the sample was dried in a vacuum oven at 60 °C overnight. For an organic semiconductor material such as an OFET channel layer, a pentacene thin film (ca. 50 nm) was deposited by a thermal evaporation method under high vacuum conditions (ca. 10–7 Torr; 1 Torr = 133.32 Pa). The deposition rate of pentacene was 0.1–0.2 Å s\(^{-1}\) while the substrate was maintained at room temperature (22 °C). This OFET memory device was completed by evaporating gold (30 nm) through a shadow mask to form the source and drain electrodes on the pentacene thin film. The device had a channel length and width of 50 μm and 2 mm, respectively. A more detailed description of the evaporation process can be found in a previous publication [26]. The electrical characteristics of the OFET memory device were measured with a KEITHLEY 4200 semiconductor characterization system in the dark and in ambient conditions at room temperature. The whole gate dielectric capacitance \(( C_i )\), measured using an Agilent 4156C capacitance–voltage measurement system at 100 kHz, was 8.4 nF cm\(^{-2}\). In addition, a quartz–tungsten–halogen lamp with a smooth spectrum in the visible range and an intensity of 5 mW cm\(^{-2}\) was used to illuminate the sample with visible light.

Received: June 28, 2006
Revised: September 4, 2006
Published online: November 10, 2006